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WHAT IS CLAIMED IS:

1. A debugging circuit capable of debugging a plurality of possible microprocessors, comprising:

a debug port;

a plurality of microprocessor sockets, each of said microprocessor sockets adapted to receive a microprocessor;

a plurality of switches, each of said plurality of switches corresponding to a respective one of said plurality of microprocessor sockets;

wherein said plurality of microprocessor sockets are adapted to form a serial signal path, and wherein each of said switches is capable of automatically detecting whether a microprocessor is present in the corresponding microprocessor socket, and if a microprocessor is present in said corresponding microprocessor socket then said switch is automatically configured to include said microprocessor within said signal path, and if a microprocessor is not present in said corresponding microprocessor socket then said switch is automatically configured so that said signal path bypasses said corresponding microprocessor socket.

2. The debugging circuit according to claim 1, wherein a debugging input is provided to each microprocessor socket, and wherein a debugging output is provided from each microprocessor that is present in said corresponding microprocessor socket.

3. The debugging circuit according to claim 2, wherein each switch receives as an input a microprocessor detection signal indicating whether said corresponding microprocessor is present.

4. The debugging circuit according to claim 3, wherein for each switch, if said microprocessor is present then said switch provides as an output said debugging output of said corresponding microprocessor.

5. The debugging circuit according to claim 4, wherein for each switch, if said microprocessor is not present, then said switch provides as a switch output said debugging input to said corresponding microprocessor.

6. The debugging circuit according to claim 5, wherein for each switch not corresponding to a last microprocessor in said serial signal path, said switch output is provided as a debugging input to a subsequent microprocessor in said serial signal path.

7. The debugging circuit according to claim 6, wherein for said switch corresponding to said last microprocessor in said serial signal path, said switch output is provided to said debug port.

8. The debugging circuit according to claim 7, wherein said debug port is electrically coupled to a computer and receives input from and provides output to said computer.

9. The debugging circuit according to claim 8, wherein said plurality of switches each comprise a pair of bipolar transistors.

10. The debugging circuit according to claim 8, wherein said plurality of switches each comprise field effect transistors.

11. A debugging switch for use in a debugging circuit capable of debugging a plurality of possible processors comprising:

a first node for receiving a processor detection signal indicating whether a first processor is present in a corresponding processor socket;

a second node for receiving a debugging input signal to said first processor;

a third node for receiving a debugging output signal from said first processor if said first processor is present in said corresponding processor socket;

a fourth node for providing a switch output signal; and

a switching element, wherein if said processor detection signal indicates that said corresponding processor is not present, then said switching element is automatically configured so that said switch provides as a switch output said debugging input signal, and wherein if said processor detection signal indicates that said corresponding processor is

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present, then said switching element is automatically configured so that said switch provides as a switch output said debugging output signal.

12. The debugging switch according to claim 11, wherein said switching element further comprises first and second bipolar transistors.

13. The debugging switch according to claim 12, wherein said switching element comprises field effect transistors.

14. The debugging switch according to claim 13, wherein said field effect transistors are junction field effect transistors.

15. The debugging switch according to claim 13, wherein said field effect transistors are insulated gate field effect transistors.

16. The debugging switch according to claim 11, wherein said switch output is provided as a debugging input to a second processor.

17. A method for debugging at least one of a plurality of possible microprocessors, comprising the steps of:

providing a debugging circuit having a plurality of microprocessor sockets adapted to form a serial signal path, wherein each microprocessor socket corresponds to a different one of said plurality of possible microprocessors and is capable of receiving a microprocessor;

providing a switch corresponding to each of said microprocessor sockets;

providing as an input to each of said switches a processor detection signal indicating whether a microprocessor is present in said corresponding microprocessor socket;

providing as an input to each of said switches a processor debugging input for said corresponding microprocessor;

providing as an input to each of said switches a processor debugging output from said corresponding processor if said microprocessor is present in said corresponding microprocessor socket;

said switch providing as a switch output said processor debugging input if said corresponding microprocessor is not present in said corresponding microprocessor socket, and providing as a switch output said processor debugging output if said microprocessor is present in said corresponding microprocessor socket.

18. The method according to claim 17, further comprising the step of:

for each switch corresponding to a microprocessor that is not a last microprocessor in said serial signal path, providing said switch output as a debugging input to a subsequent microprocessor in said serial signal path.

19. The method according to claim 18, further comprising the step of:

for said switch corresponding to said last microprocessor in said serial signal path, providing said switch output to a debug port.

20. The method according to claim 19, further comprising the step of:

providing as a debugging input to a first microprocessor in said serial signal path a signal received from said debug port.

21. The method according to claim 20, wherein said switches each comprise a pair of bipolar transistors.

22. The method according to claim 20, wherein said switches each comprise field effect transistors.